MD6301

60V Three-phase MOSFET Driver With Adaptive Dead Time and Shoot-Through Protection

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1. Features

- 6.5V to 20V Gate Drive Supply Voltage Range
- 60V VM Operating Voltage/up to 80V VBOOT
- Tolerant -7V Voltage On HS Pin
- Advanced Adaptive Dead Time
- Intelligent Shoot-Through Protection
- On-Chip Bootstrap Diode
- Fast 35ns Propagation Time
- Drives 1000pF Load with 20ns Rise and Fall Time
- 5V/50mA internal LDO
- Separate High- and Low-Side Under-voltage Protection
- Over Temperature Protection
- –40 ° C to +125 ° C Junction Temperature Range
- Available in 24-pin TSSOP package with ePAD

2. General Description

The MD6301 is an 60V 3-phase half-bridge MOSFET driver that features adaptive dead time and shoot-through protection. The adaptive dead time circuitry actively monitors the half-bridge outputs to minimize the time between high-side and low-side MOSFET transitions, thus maximizing power efficiency. Shoot-through protection circuitry prevents erroneous inputs and noise from turning both MOSFETS on at the same time.

The MD6301 also offers a wide 6.5V to 20V operating supply range to maximize system efficiency. The low 6.5V operating voltage allows longer run times in battery-powered applications. Additionally, the MD6301's adjustable gate drive sets the gate drive voltage to V_{DD} for optimal MOSFET $R_{DS(ON)}$, which minimizes power loss due to the MOSFET's $R_{DS(ON)}$.

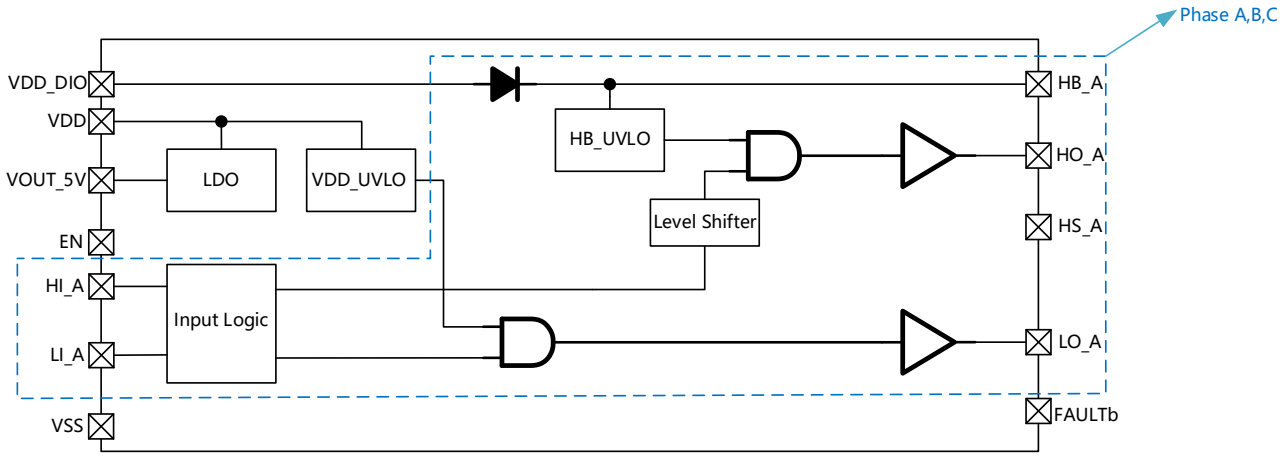
MD6301 can survive lower than -7V on HS pin during switching, so an external schottky diode is not necessary.

MD6301 integrated a 50mA/5V LDO for external circuit power supply which will minimize the PCB area and save the system cost.

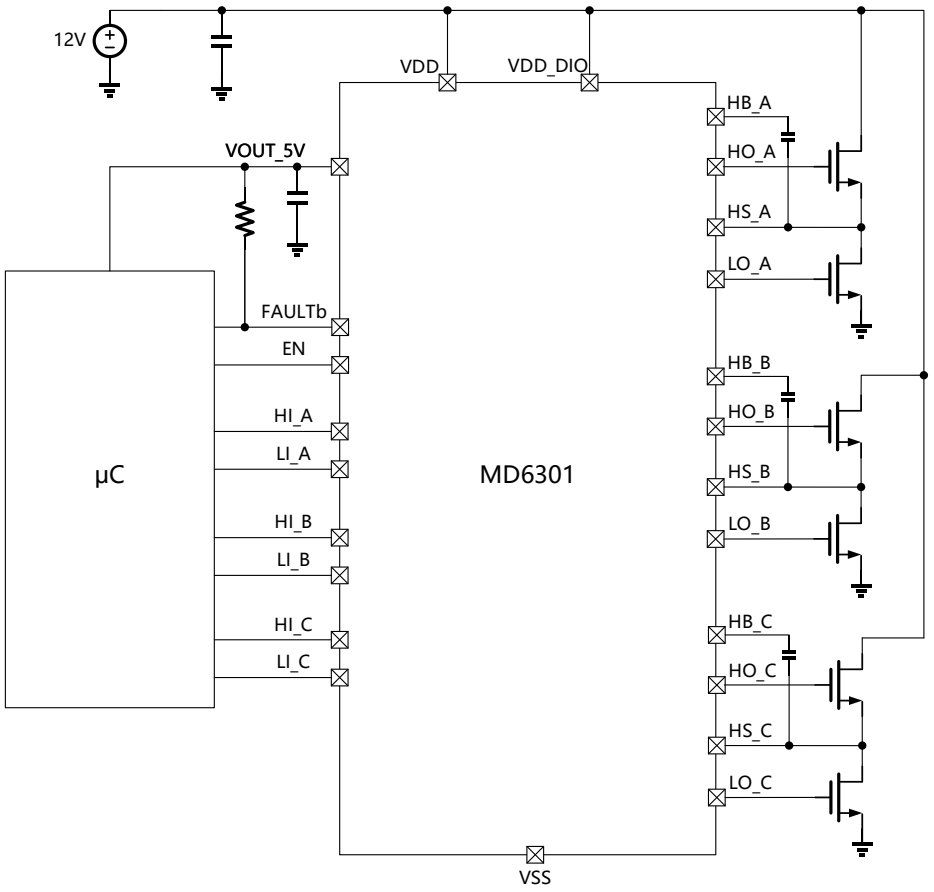
The MD6301 is available in a 24-pin TSSOP package with exposed thermal pad, the MD6301 have an operating junction temperature range of –40 ° C to +125 ° C.

3. Functional Block Diagram and Typical Application Circuit

3.1 Block Diagram

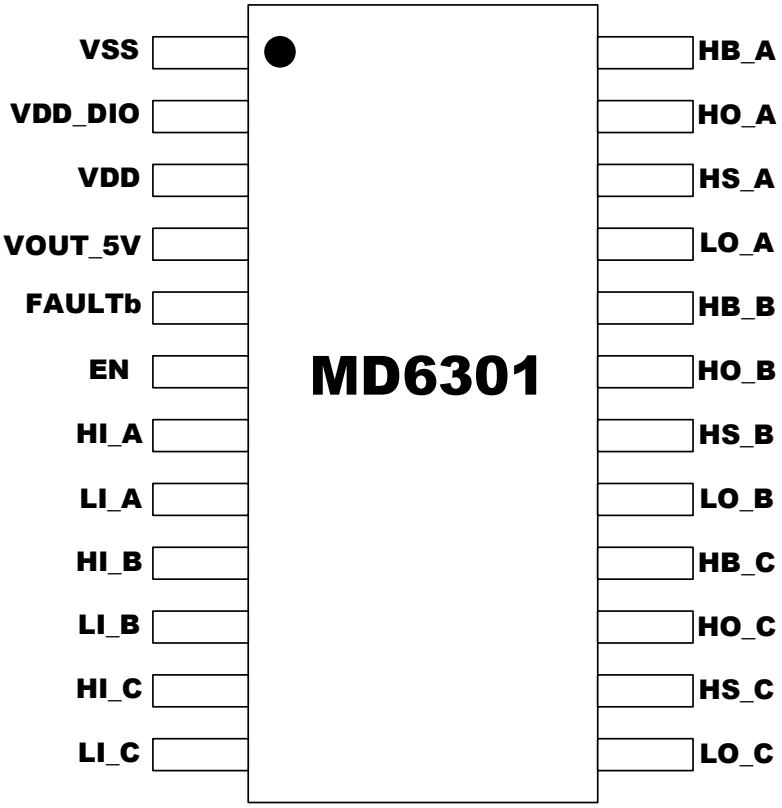


3.2 Typical Simplified Application Circuit



4. Pin Configuration

4.1. 24-Pin TSSOP(TOP VIEW)



4.2 TSSOP-24L Pin Definition

Pin No.	Pin Name	Description
7/9/11	HI_A/B/C	High Side Driver Inputs
8/10/12	LI_A/B/C	Low Side Driver Inputs
6	EN	Logic input to shutdown functionality. Logic functions when EN is high
5	FAULTb	Indicates over-temperature or low-side undervoltage lockout has occurred. This pin has negative logic and an open-drain output. Connect 5K to OUT pin.
2	VDD_DIO	Input supply for internal bootstrap diode. Decouple this pin to VSS with a >1 µF capacitor.
3	VDD	Input supply for gate drivers. Decouple this pin to VSS with a >1 µF capacitor.
4	VOUT_5V	5V LDO output, connect a 2.2uF Capacitor from this pin to VSS
1	VSS	GND
13/17/21	LO_C/B/A	Low-Side Drive Output. Connect to the gate of the external low-side power MOSFET.
14/18/22	HS_C/B/A	High-Side Drive Reference Connection. Connect to source of the external high-side power MOSFET. Connect the bottom of bootstrap capacitor to this pin.
15/19/23	HO_C/B/A	High-Side Drive Output. Connect to the gate of the external high-side power MOSFET.
16/20/24	HB_C/B/A	High-Side Bootstrap Supply. An external bootstrap capacitor is required. Connect the bootstrap capacitor across this pin and HS. An on-chip bootstrap diode is connected from VDD_DIO to HBx

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}, V_{DD_DIO}	Supply Voltage	-0.3 to +28	V
V_{LI}, V_{HI}	Input Voltage	-0.3 to 6.5	V
V_{LO}	Voltage On LO Pin	-0.3 to V_{DD}+0.3	V
V_{HO}	Voltage On HO Pin	V_{HS}-0.3 to V_{HB}+0.3	V
V_{HS}	Voltage On HS Pin Continuous	-10 to +70	V
V_{HB}	Voltage On HB Pin	+90	V
$I_{VDD\_DIO\_HB}$	Average Current in VDD_DIO to HB Diode	100	mA
ESD	HBM:1.5kΩ Series with 100pF	HBM:2000	V

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.2 Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{DD}, $V_{DD\text{-}DIO}$	Supply Voltage	+6.5 to +20	V
V_{HS}	Voltage On HS Pin	-7 to +60	V
SR	HS Slew Rate	50	V/nS
V_{HB}	Voltage On HB Pin	V_{HS}+V_{DD_DIO} Or V_{DD_DIO} -1 to V_{DD_DIO} +60	V
T_J	Junction to Operating Temperature Range	-40 to +125	° C
T_S	Storage Temperature Range	-60 to +150	

5.3 Thermal Information

Symbol	**Parameter**	**Conditions**	**Value**	**Unit**
θ_{JA}	Thermal Resistance (Junction to Ambient)	TSSOP-24L(with ePAD)		° C /W
θ_{JC}	Thermal Resistance (Junction to top Case)	TSSOP-24L(with ePAD)		° C /W

Note: Sustained junction temperatures above +125°C can impact the device reliability.

5.4 DC Electrical Characteristic

(**V_{DD}= V_{DD_DIO} =V_{HB} =12V; VSS = V_{HS}=0V; No load on LO&HO&VOUT_5V; TA= +25°C; unless otherwise noted. Bold values indicate –40°C ≤ TJ≤ +125°C.) Note 1**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	V_{DD} Quiescent Current	LI_X=HI_X=0V, EN=0V	—	60	**100**	μA
I_{DDO}	V_{DD} Operating Current	f =20 kHz	—	200	**500**	μA
I_{HB}	Total HB Quiescent Current	LI = HI =0V or LI=0V and HI=5V	—	30	**75**	μA
I_{HBO}	Total HB Operating Current	f=20 kHz	—	45	**100**	μA
I_{HBS}	HB to V_{SS} Quiescent Current	V_{HS}=V_{HB} = 60V	—	0.05	**5**	μA
LDO						
OUT	Output Voltage	V_{DD} from 6.5V to 20V, I_{OUT} =10mA	**4.85**	5.0	**5.15**	V
I_{OUT}	Max Output Current			50		mA
Input (TTL: LI_X, HI_X, EN) (Note 2)						
V_{IL}	Low-Level Input Voltage		—	—	**0.8**	V
V_{IH}	High-Level Input Voltage		**2.2**	—	—	V
V_{HYS}	Input Voltage Hysteresis		—	0.1	—	V
R_I	Input Pull-down Resistance	LI and HI and EN	**100**	300	**500**	kΩ
Under-voltage Protection & Bootstrap Diode						
V_{DDF}	V_{DD} Falling Threshold		**5.25**	5.5	**5.75**	V
V_{DDH}	V_{DD} Threshold Hysteresis		—	0.25	—	V
V_{HBF}	HB Falling Threshold		**5**	5.25	**5.5**	V
V_{HBH}	HB Threshold Hysteresis		—	0.25	—	V
V_F	Bootstrap Diode Forward Voltage	I_{VDD_DIO-HB} =100μA	—	0.64	—	V
R_D	Bootstrap Diode Dynamic Resistance	I_{VDD_DIO-HB}=5mA	—	50	—	Ω
Over Temperature Protection&FAULTb						
TSD	Over Temperature Protection Threshold			150		ºC
	Hysteresis			20		ºC
V_{FAULTb}	FAULTb Low Voltage	VDD=5V, source 1mA to FAULTb	—	56	**80**	mV
LO Gate Driver						
V_{OLL}	Low-Level Output Voltage	I_{LO}=50mA	—	0.1	**0.6**	V
V_{OHL}	High-Level Output Voltage	I_{LO}=–50mA, V_{OHL} = V_{DD} – V_{LO}	—	0.2	**1**	V
I_{OHL}	Peak Sink Current	V_{LO}=0V	—	1	—	A
I_{OLL}	Peak Source Current	V_{LO}=12V	—	1	—	A
HO Gate Driver						
V_{OLH}	Low-Level Output Voltage	I_{HO}=50mA	—	0.1	**0.6**	V
V_{OHH}	High-Level Output Voltage	I_{HO}=–50mA, V_{OHH} = V_{HB} – V_{HO}	—	0.2	**1**	V
I_{OHH}	Peak Sink Current	V_{HO}=0V	—	1	—	A
I_{OLH}	Peak Source Current	V_{HO}=12V	—	1	—	A

5.5 Switching Electrical Characteristic

(V_{DD}= V_{DD_DIO} =V_{HB} =12V; VSS = V_{HS}=0V; No load on LO&HO&VOUT_5V; TA= +25°C; unless otherwise noted. **Bold** values indicate –40°C ≤ TJ≤ +125°C.**)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
(LI/HI mode with inputs non-overlapping, assumes HS low before LI goes high and LO low before HI goes high)						
t_{LPHL}	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	—	—	35	**75**	ns
t_{HPHL}	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	—	—	35	**75**	ns
t_{LPLH}	Lower Turn-On Propagation Delay (LI Rising to LO Rising)	—	—	35	**75**	ns
t_{HPLH}	Upper Turn-On Propagation Delay (HI Rising to HO Rising)	—	—	35	**75**	ns
$t_{RC/FC}$	Output Rise/Fall Time	C_L=1000pF	—	20	—	ns
$t_{R/F}$	Output Rise/Fall Time (3V to 9V)	C_L=0.1μF	—	0.8	—	μs
t_{PW}	Minimum Input Pulse Width that Changes the Output		—	50	—	ns
V_{LOOFF}	LO Output Voltage Threshold for LO FET to be Considered Off			1.5		V
V_{SWTH}	Switch Node Voltage Threshold Signaling HO is Off			1.8		V

Note1: Specifications are for packaged product only.

Note2: $V_{IL(MAX)}$ = maximum positive voltage applied to the input which will be accepted by the device as a logic low.

$V_{IH(MIN)}$ = minimum positive voltage applied to the input which will be accepted by the device as a logic high.

5.6 Typical Characteristic(need update)

(V_{DD}=V_{HB} =12V; VSS = VHS=0V; No load on LO or HO; T_A= +25°C; unless otherwise noted. **Bold** values indicate –40°C ≤ T_J≤ +125°C.**)**

Figure 5-1: Quiescent Current VS Temperature

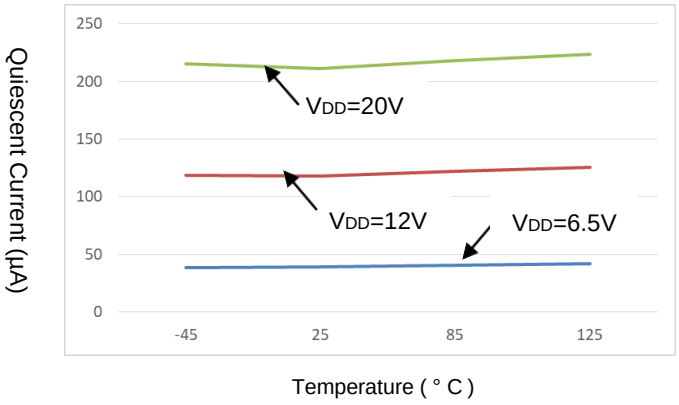


Figure 5-2: Operation Current VS Temperature

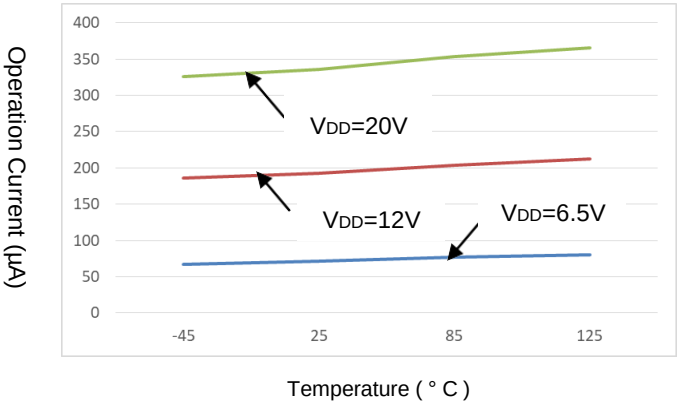


Figure 5-3: Low Side Input / Output (LI/LO)

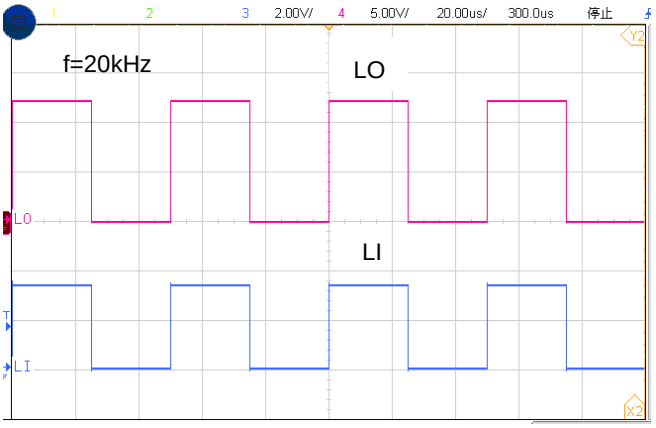


Figure 5-4: High Side Input / Output (HI/HO)

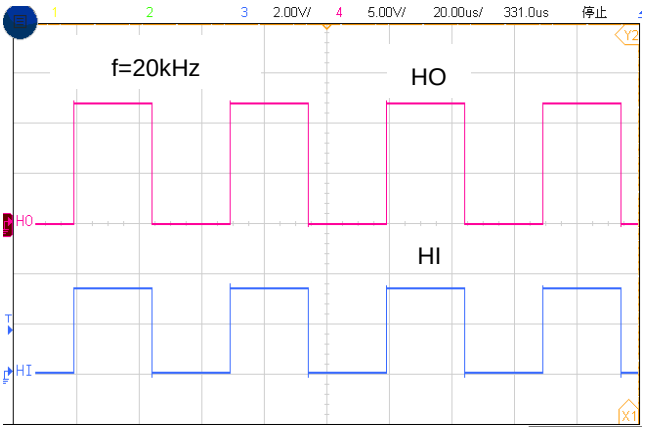


Figure 5-5: T_{LPLH} Delay

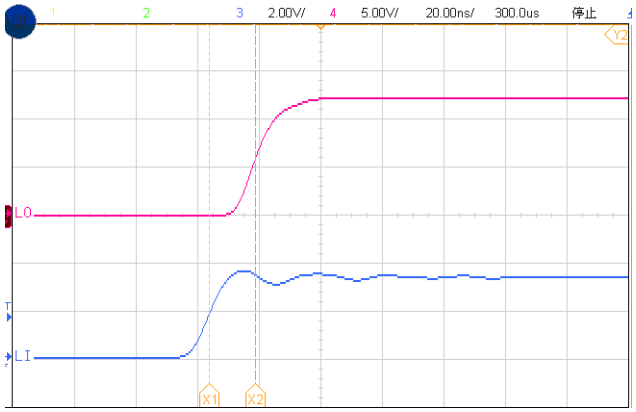
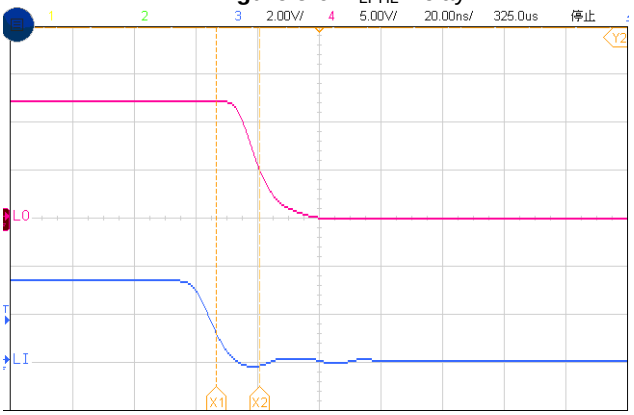


Figure 5-6: T_{LPHL} Delay



6. Device Operation

6.1 Timing Diagram

The external LI/HI inputs are delayed to the point that HS is low before LI is pulled high and similarly, LO is low before HI goes high. HO goes high with a high signal on HI after a typical delay of 35ns (t_{HPLH}). HI going low drives HO low, also with a typical delay of 35ns (t_{HPHL}). Likewise, LI going high forces LO high after a typical delay of 35ns (t_{LPLH}) and LO follows the low transition of LI after a typical delay of 35ns (t_{LPHL}). HO and LO output rise and fall times (t_R/t_F) are typically 20ns, driving 1000pF capacitive loads.

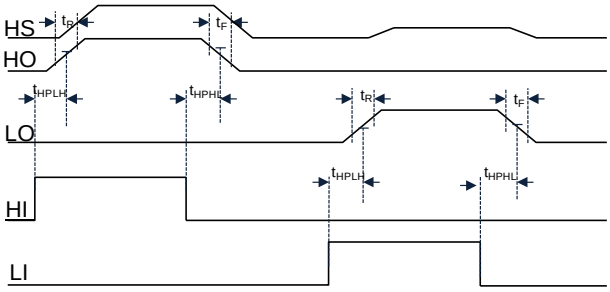


Figure 6-1: Separate Non-Overlapping LI/HI Input Mode

(All propagation delays are measured from the 50% voltage level)

When the LI/HI input on conditions overlap, LO/HO output states are dominated by the first output to be turned on. That is, if LI goes high (on) while HO is high, HO stays high until HI goes low; at which point, after a delay of t_{HOOFF} and when HS < 1.8V, LO goes high with a delay of t_{LOON}. Should HS never trip the aforementioned internal comparator reference (1.8V), a falling HI edge delayed by 250ns will set the “HS latch”, allowing LO to go high. If HS falls very fast, LO will be held low by a 35 ns delay gated by HI going low. Conversely, HI going high (on) when LO is high has no effect on the outputs until LI is pulled low (off) and LO falls to < 1.5V. Delay from LI going low to LO falling is t_{LOOFF} and delay from LO < 1.5V to HO being on is t_{HOON}.

The PWM signal applied to the MD6301 going low causes HO to go low, typically 35ns (t_{HOOFF}) after the PWM input goes low; at which point, the switch node HS falls.

When HS reaches 1.8V (V_{SWTH}), the external high-side

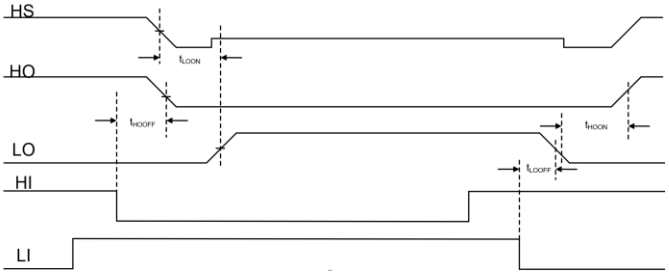


Figure 6-2: Separate Overlapping LI/HI Input Mode

MOSFET is deemed off and LO goes high, typically within 35ns (t_{LOON}). HS falling below 1.8V sets a latch that can only be reset by PWM going high. This design prevents ringing on HS from causing an indeterminate LO state. Should HS never trip the aforementioned internal comparator reference (1.8V), a falling PWM edge delayed by 250ns will set the “HS latch”, allowing LO to go high. An 80ns delay, gated by PWM going low, may determine the time to LO going high for fast falling HS designs (3-4 in Figure 6-3). PWM goes high forcing LO low in typically 35ns (t_{LOOFF}) (5-6 in Figure 6-3). When LO reaches 1.5V (V_{LOOFF}), the low-side MOSFET is deemed off and HO is allowed to go high. The delay between these two points is typically 35ns (t_{LOON}). HO goes high with a high signal on HI after a typical delay of 35ns (t_{HPLH}). HI going low drives HO low, also with a typical delay of 35ns (t_{HPHL}) (7-8 in Figure 6-3). HO and LO output rise and fall times (t_R/t_F) are typically 20ns, driving 1000pF capacitive load.

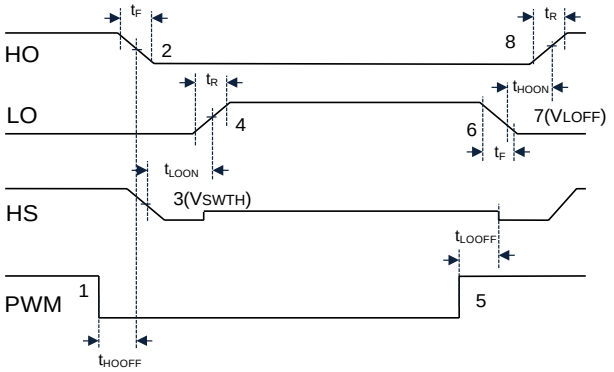


Figure 6-3: PWM Mode

(All propagation delays are measured from the 50% voltage level)

For HO to be high, HI must be high and LO must be low. HO going high is delayed by LO falling below 1.5V. The HI and LI inputs must not rise at the same time to prevent a glitch from occurring on the output. A minimum 50ns delay between both inputs is recommended. LO is turned off very quickly on the LI falling edge. LO going high is delayed by the longer of a 35 ns delay of the HO control signal going "off" or the RS latch being set. The latch is set by the quicker of either the falling edge of HS or the LI gated delay of 240 ns. The latch is present to lockout LO bounce due to ringing on HS. If HS never adequately falls due to the absence of or the presence of a very weak external pull-down on HS, the gated delay of 240 ns at LI will set the latch, allowing LO to transition high. This, in turn, allows the LI start-up pulse to charge the bootstrap capacitor if the load inductor current is very low and HS is uncontrolled. The latch is reset by the LI falling edge.

Other Timing Considerations:

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input. The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the CB capacitor to charge during the off-time. Adequate time must be allowed for the CB capacitor to charge up before the high-side driver is turned on.

6.2 Start-up and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

6.3 Enable Input

Logic high on the enable pin (EN) allows for start-up and normal operation to occur. Conversely, when a logic low is applied on the enable pin, the device enters Shutdown mode.

6.4 Input Stage

Both the HI/LI pins of the MD6301 is referenced to the VSS pin. The voltage state of the input signal(s) does not change the quiescent current draw of the driver. The MD6301 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the VDD supply voltage andthere is no dependence between VDD and the input signal amplitude with the MD6301. This feature makes the MD6301 an excellent level translator that will drive high-threshold MOSFETs from a low-voltage PWM IC.

6.5 Low-Side Driver

A block diagram of the low-side driver is shown in Figure 6-4. The low-side driver is designed to drive a ground (VSS pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{DS(ON)}$ from the external MOSFET. A high level applied to the LI pin causes the upper driver MOSFET to turn on and VDD voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low-side driver to ground the gate of the external MOSFET.

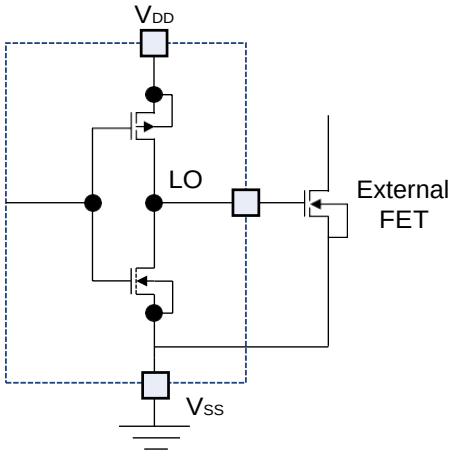


Figure 6-4: Low-Side Driver

6.6 High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 6-5. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

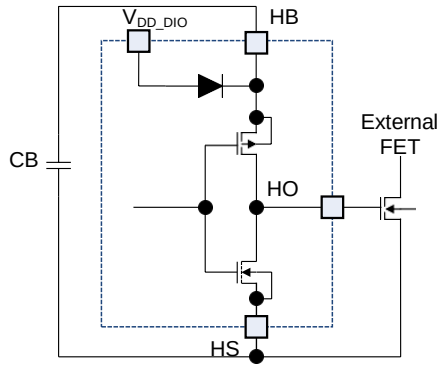


Figure 6-5: High-Side Driver and Bootstrap Circuit

A low-power, high-speed, level-shifting circuit isolates the low-side (VSS pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit, while the voltage level of the HS pin is shifted high. The bootstrap circuit consists of an internal diode and external capacitor, CB. In a typical application, such as the synchronous buck converter shown in Figure 6-6, the HS pin is at ground potential while the low-side MOSFET is on. The internal diode allows capacitor CB to charge up to $V_{DD\_DIO} - V_F$ during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the HO pin turns on, the voltage across capacitor CB is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HS pin rises with the source of the high-side MOSFET until it reaches VIN. As the HS and HB pins rise, the internal diode is reverse biased, preventing capacitor CB from discharging.

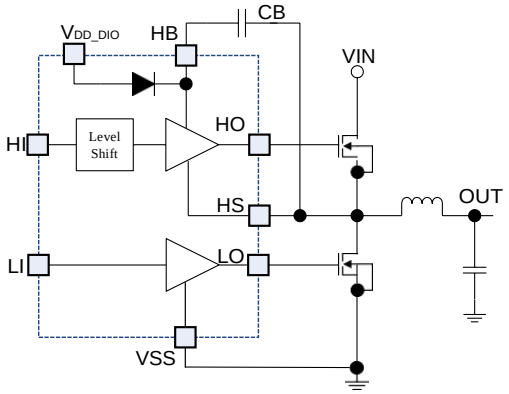


Figure 6-6: Synchronous Buck Converter

6.7 FAULT Indicator

A 5K ohms resistor is connected between FAULTb and VOUT_5V, FAULTb will be pulled low when V_{DD} UVLO or TSD event happens.

6.8 Adaptive Dead Time

It is important that only one of the two MOSFETs is on at any given time. If both MOSFETs on the same side of the half-bridge are simultaneously on, VIN will short to ground. The high current from the shorted VIN supply will then "shoot through" the MOSFETs into ground. Excessive shoot-through causes higher power dissipation in the MOSFETs, voltage spikes and ringing in the circuit. The high current and voltage ringing generate conducted and radiated EMI. Table7-1 illustrates truth tables that details the"first on" priority as well as the failsafe delay.

Table 7-1

LI	HI	LO	HO	Comments
0	0	0	0	Both outputs off
0	1	0	1	HO will not go high until LO falls below 1.5V
1	0	1	0	LO will be delayed an extra 240ns if HS never falls below 1.8V
1	1	x	x	First on stays on until input of same goes low

Minimizing shoot-through can be done passively, actively or through a combination of both. Passive shoot-through protection can be achieved by implementing delays between the high and low gate drivers to prevent both MOSFETs from being on at the same time. These delays can be adjusted for different applications. Although simple, the disadvantage of this approach is that it requires long delays to account for process and temperature variations in the MOSFET and MOSFET driver.

Adaptive dead time monitors voltages on the gate drive outputs and switch node to determine when to switch the MOSFETs on and off. This active approach adjusts the delays to account for some of the variations, but it too has its disadvantages. High currents and fast switching voltages in the gate drive and return paths can cause parasitic ringing to turn the MOSFETs back on, even while the gate driver output is low. Another disadvantage is that the driver cannot monitor the gate voltage inside the MOSFET. Figure 6-7 shows an equivalent circuit of the gate driver section, including parasitics.

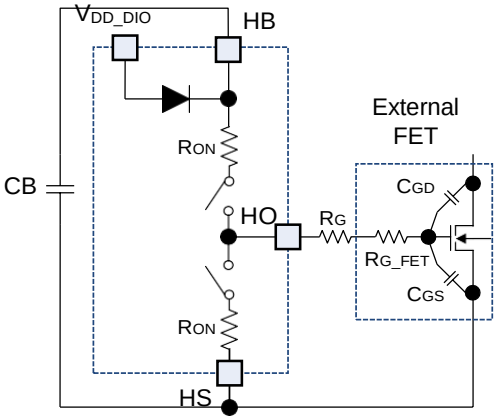


Figure 6-7: MD6301 Driving an External MOSFET

The internal gate resistance (RG_FET) and any external damping resistor (RG) isolate the MOSFET's gate from the driver output. There is a delay between when the driver output goes low and the MOSFET turns off. This turn-off delay is usually specified in the MOSFET data sheet. This delay increases when an external damping resistor is used. The MD6301 uses a combination of active sensing and passive delay to ensure that both MOSFETs are not on at the same time, minimizing shoot-through current. Figure 6-8 illustrates how the adaptive dead-time circuitry works.

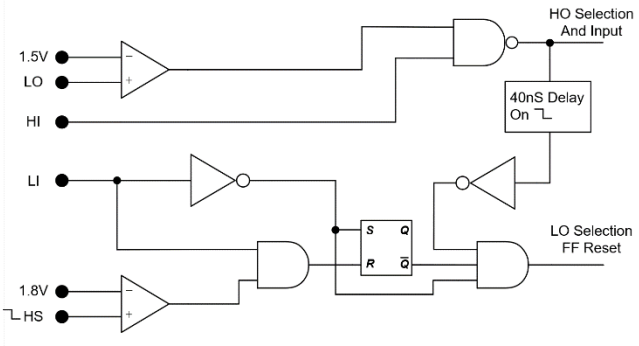


Figure 6-8: Adaptive Dead-Time Logic Diagram (PWM)

Figure 6-9 shows the dead time (<35ns) between the gate drive output transitions as the low-side driver transitions from on to off, while the high-side driver transitions from off to on.

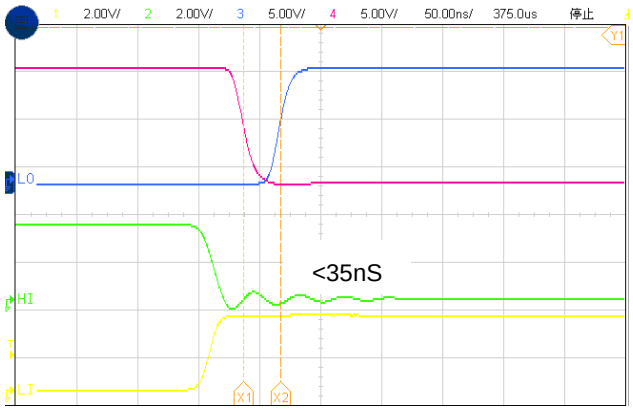


Figure 6-9: Adaptive Dead-Time LO (Low) to HO (High)

A high level on the PWM pin causes the LO pin to go low. The MD6301 monitors the LO pin voltage and prevents the HO pin from turning on until the voltage on the LO pin reaches the V_{LOOFF} threshold. After a short delay, the MD6301 drives the HO pin high. Monitoring the LO voltage eliminates any excessive delay due to the MOSFET drivers turn-off time, and the short delay accounts for the MOSFET turn-off delay, as well as letting the LO pin voltage settle out. An external resistor between the LO output and the MOSFET may affect the performance of the LO pin monitoring circuit and is not recommended. A low on the PWM pin causes the HO pin to go low after a short delay (t_{HOOFF}). Before the LO pin can go high, the voltage on the switching node (HS pin) must have dropped to 1.8V.

Monitoring the switch voltage instead of the HO pin voltage eliminates timing variations and excessive delays due to the high-side MOSFET turn-off. The LO driver turns on after a short delay (t_{LOON}). Once the LO driver is turned on, it is latched on until the PWM signal goes high. This prevents any ringing or oscillations on the switch node, or the HS pin from turning off the LO driver. If the PWM pin goes low and the voltage on the HS pin does not cross the VSWTH threshold, the LO pin will be forced high after a short delay (t_{SWTO}), ensuring proper operation. Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase-shift errors in power supplies with wide bandwidth control loops.

Care must be taken to ensure that the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input. The maximum duty cycle (ratio of high-side on-time to switching period) is determined by the time required for the CB capacitor to charge during the off-time. Adequate time must be allowed for the CB capacitor to charge up before the high-side driver is turned back on. Although the adaptive dead-time circuit in the MD6301 prevents the driver from turning both MOSFETs on at the same time, other factors outside of the antishoot-through circuit's control can cause shoot-through. Other factors include ringing on the gate drive node and capacitive coupling of the switching node voltage on the gate of the low-side MOSFET.

6.9 HS Pin Clamp

A resistor/diode clamp between the switch node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin. Figure 6-10 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three-phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side

MOSFET is conducting during the On-Time state, current flows into the motor. After the high-side MOSFET turns off, but before the low-side MOSFET turns on, current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current. Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and possibly a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 7V, a diode or a Schottky diode between the HS pin and ground is recommended. The diode reverse voltage rating must be greater than the high-voltage input supply (VIN). Larger values of resistance can be used if necessary. Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

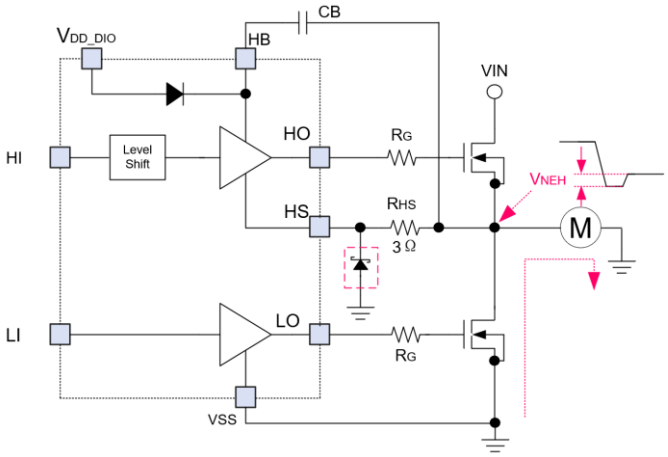


Figure 6-10: Negative HS Pin Voltage

6.10 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the CB capacitor, multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode. An optional external bootstrap diode may be used instead of the internal diode (Figure 6-11). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the VDD supply voltage.

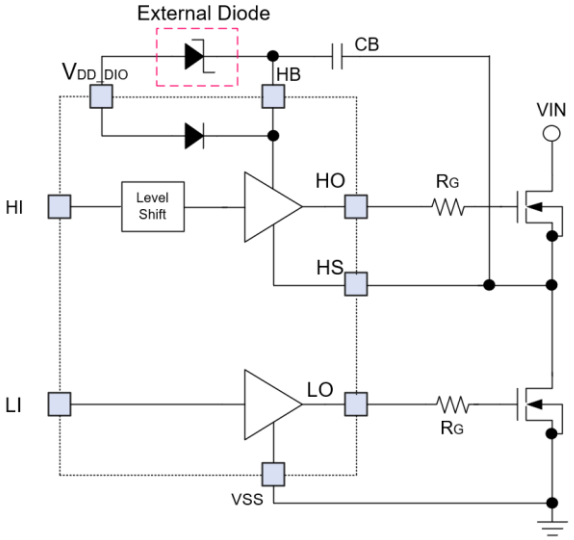


Figure 6-11: Optional Bootstrap Diode

6.11 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (V_{DD}) and high-side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U-type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1 µF is required for each of the capacitors, regardless of the

MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low-voltage capacitors are used, because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage. Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and VSS pins. The bypass capacitor (CB) for the HB supply pin must be located as close as possible between the HB and HS pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as below equation:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

- Q_{GATE}=*Total Gate Charge at* V_{HB}
- ΔV_{HB}=*Voltage Drop at HB Pin*

The decoupling capacitor for the V_{DD} input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

If large bootstrap capacitors (over 220nF) are used, the pre-charge done with multiple pulses at a 20% duty cycle is recommended to limit the amount of power dissipated in the bootstrap diodes.

6.12 Grounding and Component Placement

Nanosecond switching speeds and ampere peak currents in excessive ringing or circuit latch-up. Figure 6-12 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low-impedance ground plane.

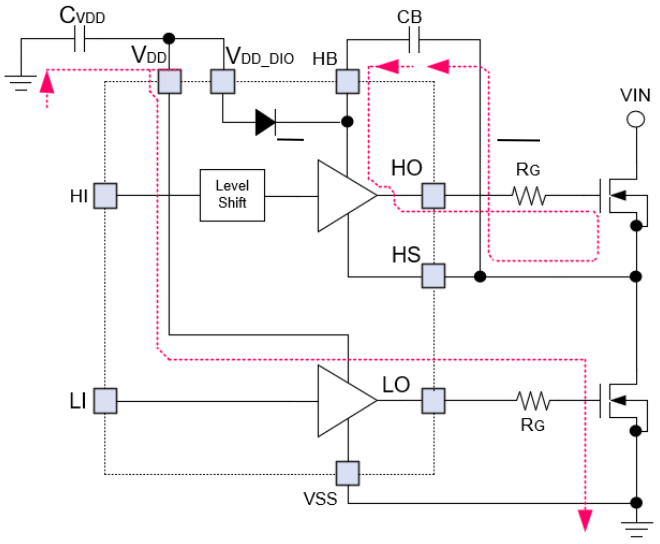


Figure 6-12: Turn-On Current Paths

Charge needed to turn on the MOSFET gates comes from the decoupling capacitors, C_{VDD} and CB. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on. Current in the high-side driver is sourced from and around the MD6301 drivers require proper placement and trace routing of all components. Improper placementmay cause degraded noise immunity and false switching, capacitor CB and flows into the HB pin and out the HO pin, into the gate of the high-side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor CB. The high-side circuit return path usually does not have a low-impedance ground plane, so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that

fights the turn-on of the MOSFET. It is important to note that capacitor CB must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on, but it must also keep HB pin noise and ripple low for properoperation of the high-side drive circuitry.

Figure 6-13 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in thebootstrap capacitor CB.

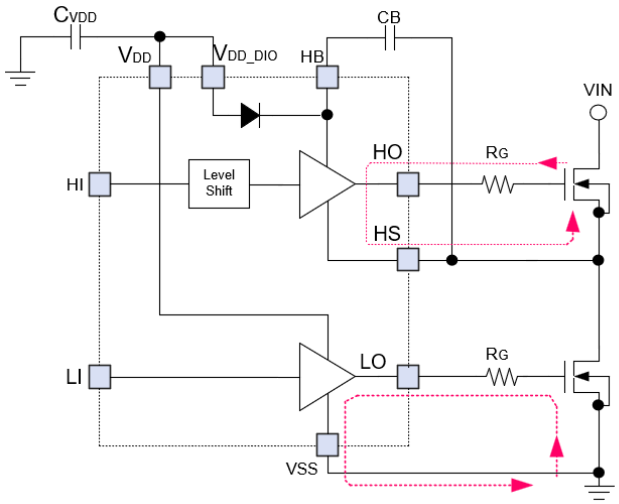
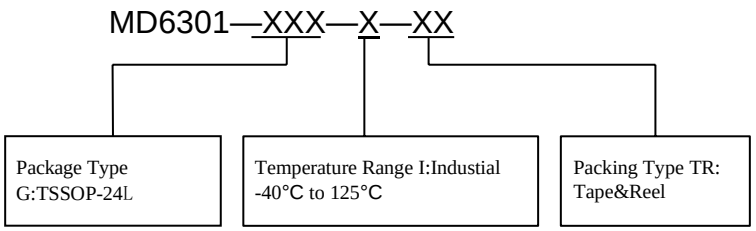


Figure 6-13: Turn-Off Current Paths

7. Ordering Information



Part Number	Package Type	Packing Information	
MD6301XI-TR	TSSOP-24L with ePAD	Tape & Reel	13” 2500/Reel

8. Top Markings

8.1 TSSOP-24L Package

First Line: Part Name

LOTNUMBER: Lot Number

YYWWSW：Date Code

9. Package Information

9.1 TSSOP-24L with ePAD

10. Revision History

Revision	Date	Descriptions